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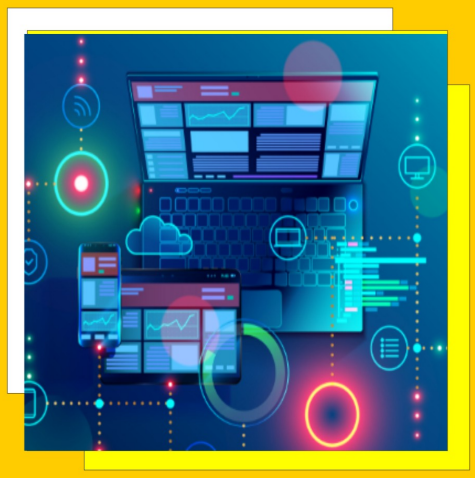

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Syllabus

Chapter	Name
I	**C.P.U Organization & Design** Topics: Machine Instructions and Addressing Modes ALU and Data Paths
II	**MicroProgrammed Control Unit** Topics: Design and Applications of Hardware and MicroProgrammed Control Unit
III	**Input – output Organization** Topics : I/O Interface; (Interrupt & DMA); Serial Communication interface
IV	**Pipelining** Topics: Parallel Processing; Pipelining types and Applications; RISC & CISC
V	**Memory Organization** Topics: Cache Memory, Main Memory, Secondary Storage Memory and Memory Interfacing
VI	**Computer Arithmetic** Topics : Fixed and floating point operations and booth multiplication

CONTENT

CHAPTER-1

CPU ORGANIZATION & DESIGN

CPU (Central Processing Unit) is made up of three major parts:

1. Arithmetic and Logic Unit (ALU)
2. Control Unit (CU) and
3. Processing Registers

- **ALU** is used to perform the required Arithmetical and logical operation under the directions of control unit.
- **Control Unit** supervises the transfer of information among the Registers and instructs the ALU that which operation has to be perform.
- **Processing Registers** are used to store the data during execution
- **The Computer instruction set** provides the specifications for the design of the CPU.

Control Word: It is a binary word that is generated by the CPU to perform one of the various operations.

Control Register: It is used to store the control word.

- If the length of the control word is n bit, total no. of operations that can be used to perform 2^n ; ranges from 00----0 (n) to 1-----1(n) and each combination is used to assign one operation.

Microoperation : It is an operation executed on data stored in registers. Micro operation is a basic register to register operation.

- Instruction is divided into 2 parts:
  1. Operation part (most side)
  2. Operand part (least side).
- For 'n' address bit CPU total no. of memory location to be accessed is 2^n and each memory location is able to store 1 word.
- Length of the word varies from one CPU to other and depends on the no. of data bits that can be transferred at a time (i.e. word size is equal to the no. of data bits a CPU has)
- The total memory is divided in to 2 parts namely
  1. User memory 2.Stack memory
- User memory is under the control of only user, but stack memory is under the control of both CPU and user.

Different ways for performing the Arithmetical operations:

1. Infix notation (Ex : A+B)
2. Prefix or polish (Ex : +AB)
3. Reverse polish notation (Postfix) (Ex: AB+)

Stack works on postfix.

Conversion of Infix to RPN

Ex: 1 $\Rightarrow A \times B + C \times D$

$= (AB\times) + (CD\times) = AB \times CD \times +$

Ex: 2 $(A+B)\times[C(D+E)+F]$

First complete the inner side of parenthesis

$= (AB+)[C\times(DE+)+F]$

$= (AB+)[DE+C\times F+] = AB+DE+C\times F+\times$

$= (AB\ +)[(CDE\ +)\ \times F]+$

$= (AB\ +)[CDE\ +F\ \times]$

$= AB\ +CDE\ +F\ \times\ +$

Conversion of RPN to Infix

Ex:1 $AB\times CD\times +$

$= (AB\times)+(CD\times)$

$= (A\times B)+(C\times D)$

$= AB+CD$

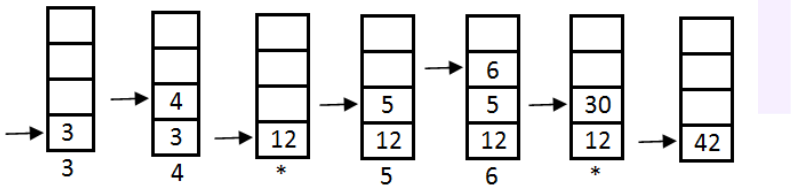
Ex: 2 $AB+DE+C\times F+\times$

$= (A+B)\times[C(D+E)+F]$

- RPN is used in some electronic calculators
- Before evaluating the operation, the arithmetic expression must be converted into RPN, the operations are pushed on to stack in the order in which they appear.
- Numerical example : for the data $(3\times4)+(5\times6)$ using RPN

$34\times56\times+$

Stack operations :



Compliers generally works on polish notation.

- In scientific calculators, some operations are performed with RPN and others with polish notation.
- The bits of the instructions are divided into 2 fields, called as Operation field and Operand field.
- Again operand field is divided in to
  1. Address field
  2. Mode field.
- Operands residing in the memory are specified by their memory address
- Operands residing in the processing Registers are specified with a Register address (name)
- In any system; if k bits are used to specify the address of the Register, then the same CPU has 2^k no. of registers (max. no.)
- The no. of address fields in the instruction format of a computer depends on the internal organization of its registers.

Instruction Cycle:

It shows the execution sequence of an instruction. It consists of two sub cycles.

1) Fetch cycle
2) Execution cycle

Instruction fetch operation takes place in the fetch cycle. Process of transferring a binary sequence using program counter from memory to CPU called as instruction fetch.

At the end of instruction fetch program counter is incremented to next instruction address.

$$PC \rightarrow \overset{Memory}{\boxed{Binary\ seq.}} \rightarrow C.P.U$$

$$PC \rightarrow PC + \text{step size}$$

After transferring a binary sequence to the CPU execution cycle is trying to process the instruction. To process the instruction there is a need of identifying the associated operation. Type of operation is identified by OPCODE.

OPCODE information is given by instruction format.

CPU Organization:

Classification is done on the basis of internal storage.

1) Stack organization
2) Accumulator based machine
3) General register organization

1) Stack organization:

- It uses push & POP instructions.
- Instruction format - $\boxed{op-code}$
- Push 'x' means, the word at the address of the 'x' is pushed to the top of the stack memory.
- In this operation, instruction does not use an address field in the stack organized computer, because the specified operation is performed on the two items that are on the top of the stack.
- It is a storage device that stores the information in such a manner that the item stored last is the first item to retrieve. Means LIFO (Last in first out)
- The register that holds the address of the stack is known as stack pointer.
- Push and pop are used to access stack memory.
- For accessing 2^n words stack memory, the length of the (stack pointer) required is 'n' bits.
- Always, SP is pointed at top of the stack; it is decremented during push operation and incremented during pop operation because the stack grows downwards.
- In 8085 for pushing → pre decrement and for poping → post increment
- 2 flags are used to know the status of the stack: 1. Empty 2. Full
- Initially, stack cleared to '0'. So EMPTY is set and Full is cleared.
- If all memory locations are filled in the stack; then empty flag resets and Full flag sets.
- But most computer do not provide hardware for checking over flow (Full stack) or under flow (empty stack); In this case the stack limits can be checked by using 2 processing Registers.
- One to hold the upper limit and other to hold the lower limit address
- After PUSH operation; SP is compared with the upper limit Register (SP is stack pointer)
- After POP operation SP is compared with the lower limit register

2) Accumulator based machine: (Advantage: length of the opcode is low, so it can be executed at faster rate.)

- ☞ In this all operations are performed with an implied accumulators
- ☞ It has only one address field. Instruction format:

→

$op-code$	$Address$

Ex: ADD x
SUB x where 'x' is the address of the operand

3) General Register organization: (Length of the OP code is more)

The instruction format needs 3 Register address fields or 2 Register address fields.

Ex: ADD R1, R2, R3
R1=R2+R3

☞ For data transfer MOV operations, it requires 2 no. Registers.

Ex: MOV R1, R2
For Arithmetical; 3 Register Required
For Data transfer; 2 Register Required

Depending on the length of the operand, instructions are divided as follows:

Instruction based on number of addresses
There are 5 type of instruction based on address:

(i) 4 – address instruction
(ii) 3 – address instruction
(iii) 2 – address instruction
(iv) 1 – address instruction
(v) 0 – address instruction.

(i) 4 – address instruction

In the 4 – address instruction, we have to specify 4-address, in which first address that is close to OP code determines the result and the last address determines the address of the next instruction.

For example: ADD A1 A2 A3 A4
In this we perform the addition of M[A2] and M[A3] and the result is stored in M[A1]. Here A4 contains the address of next **instruction.**

(ii) **3 – address instruction**

In the 3 – address instruction, we have to specify 3 – address in which the first address that is close to OP code determines the result of operation.

Example:
ADD A1, A2 A3
First we performed the M[A2] + M[A3]
Next move the reject to A1.
M[A1] ← M[A2] + M [A3]

(iii) 2-address Instruction

In the case of two – address instruction, the accumulator is used to store the result.

Example:
ADD X, Y
It represents
AC: X + Y

→ In the 2 – address instruction another position is there without using accumulator for example:

ADD X, Y
It can be performed as:
X: = X + Y

→ The addition operation stored the result into X.

(iv) 1-address instruction

→ In the one – address instruction we use accumulator. The unspecified operands are assumed to be stored in AC (Accumulator)

For example:
ADD X
It performed as
AC: = AC + X

(v) 0 – address instruction

→ A few computers name teen designed so that most instruction contain no explicit address; they can be called as zero – address machine

→ All operands used by a zero address instruction are required to be in the top location in the stack.

Example: ADD
That causes the top two operands which should be X and Y, to be removed from the stack and addressed the resulting sum X + Y is then placed at the top of the stack.

Addressing Modes

- ☞ It is the way of locating the data in the operand field.
- ☞ The control unit of a computer is designed to go through the instruction cycle that is divided into 3 major phases (steps)
  1. Fetch the instruction from memory
  2. Decode the instruction and Execution
- ☞ Program counter is used to store the address of the next instruction to be executed, and it is incremented each time by step size to point the next instruction.
- ☞ The step size depends on length of instruction.
- ☞ Decoding done in step 2 determines the operation to be performed and addressing mode of the instruction.
- ☞ Then computer executes the instruction and returns to the step 1 to fetch the next instruction.

So, to know about the functions of decoding unit, it is compulsory to know about the addressing modes.

Different Addressing Modes (AM)

Implied AM: It has no operand field

Eg: CMA, HLT, NOP, and

All zero address instruction

It is also known as implicit (AM)

Immediate AM: In this addressing mode operand part is nothing but data. This AM is used to access the constants.

These are useful for initializing Register for constant values

Ex: MOVI AX, 1234H, Add γ_0 #23 [# and I Denotes Immediate AM].

Register AM: In this operand field must be specified with Register

Ex: 1.MOV AX, BX 2. ADD, CX, DX

Register indirect: In this, the specified register stores the effective address of the operand.

Ex: MOV AX, [BX]
ADD AX, [BX]

In this example BX register is used to store the address of the operand i.e. content of the BX register acts as **Effective Address (EA)**

Effective address is an address where data is available

Direct Addressing mode: In this EA=Address of the instruction (In branch type instruction, the address field specifies the actual branch address)

Ex: MOV AX,[5555H]
JMP 2500H

Indirect addressing mode: In this mode, the effective address of the operand is stored in the memory location specified in the instruction.

Relative Addressing mode: In this, the content of the pc is added to the address part of the instruction in order to obtain the effective address

Ex: ADD AX,[+25,BX] EA=BX+25

Indexed Addressing mode: In this mode the content of the Index register is added to the address part of the instruction to obtain the EA.

☞ Index Register is a special CPU register.

Auto increment or Auto decrement Addressing mode: This is similar to the indirect mode except that the register is incremented or decremented after its value is used to access memory. This mode is used to Access the Linear Array Elements.

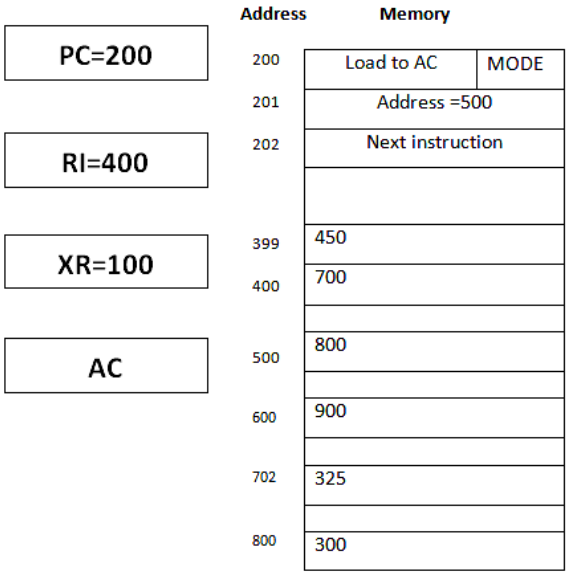
Ex:- (R) +

Here, first the content of register R is accessed and taken as effective address of the operand. After that, the content of R is incremented.

Base Register Addressing Mode: In this mode the content of a base register is added to that address part of the instruction to obtain the effective address.

This is similar to the index AM except that the register is now called a base register instead of an Index register.

NOTE: It is same as the register indirect mode except that is incremented to 401 after the instruction execution but in Auto decrement mode it is decremented prior to the execution.



Addressing Mode	Effective Address	Content of AC
Direct address	500	800
Immediate operand	201	500
Indirect address	800	300
Relative address	702	325
Indexed address	600	900
Register	-	400
Register Indirect	400	700
Auto increment	400	700
Auto decrement	399	450

Q. Which of the following is/are true of the auto-increment addressing mode?

I. It is useful in creating self-relocating code.
II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.
III. The amount of increment depends on the size of the data item accessed.
A. I only **B. II only** **C. III only** **D. II and III only**

Ans: C

EXP:

In auto-increment addressing mode the address where next data block to be stored is generated automatically depending upon the size of single data item required to store.

Self-relocating code takes always some address in memory and statement says that this mode is used for self-relocating code

So, option 1 is incorrect and no additional ALU is required.

So option (C) is correct option.

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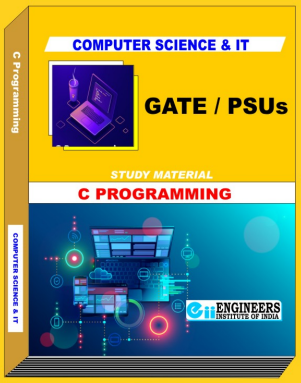

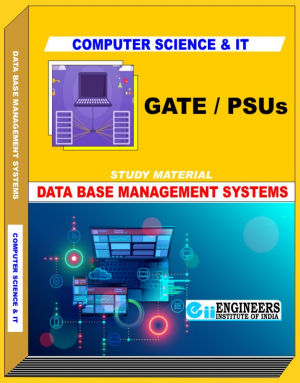

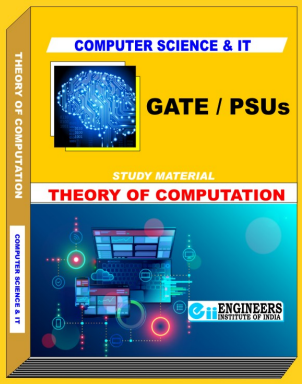

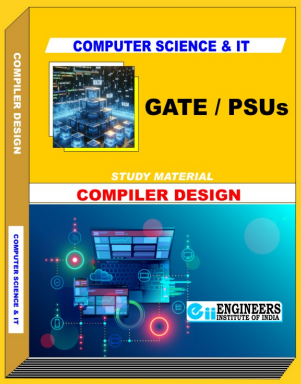

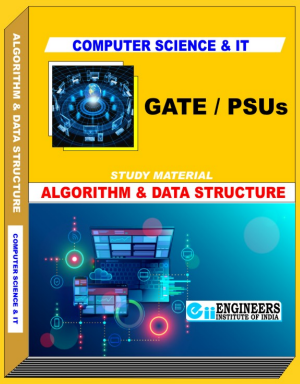

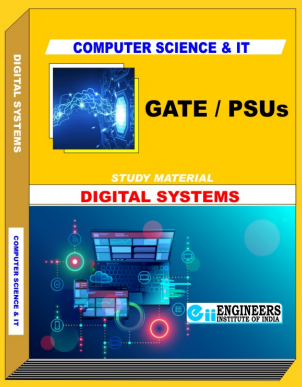

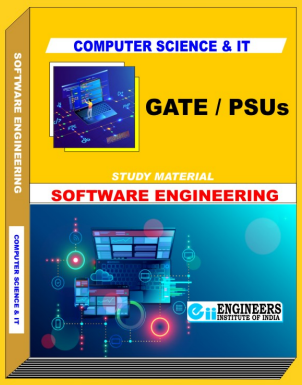

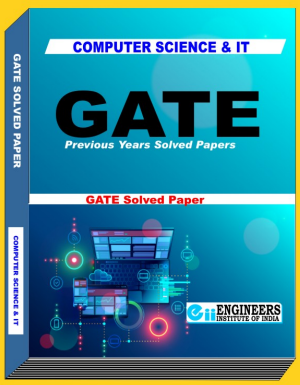

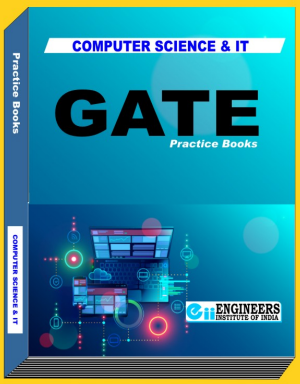

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